WHAT IS CLAIMED IS:

1. A method for fabricating MOS transistors, the method comprising the steps of:

forming a buffer oxide layer on a semiconductor substrate having an isolation layer;

conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer.

2. A method for fabricating MOS transistors, the method comprising the steps of:

forming a buffer oxide layer on a semiconductor substrate having an isolation layer;

conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer;

removing the buffer oxide layer;

forming a sacrificial layer of the semiconductor substrate;

patterning the sacrificial layer to form a trench defining a gate electrode forming region;

conducting ion implantations for threshold voltage

adjustment and punch stop formation on the semiconductor substrate area exposed by the trench;

forming a gate oxide layer on the surface of the substrate under the bottom face of the trench;

forming a polysilicon layer on the sacrificial layer so as to completely bury the trench;

polishing the polysilicon layer until the surface of the sacrificial layer is exposed, so as to form a gate electrode;

removing the sacrificial layer;

forming an LDD region in the surface of the substrate at both side portions of the gate electrode;

forming spacers on both side walls of the gate electrode; and

forming the source/drain regions in the surface of the substrate at both side portions of the gate electrode including the spacers.

3. The method for fabricating MOS transistors as claimed in claim 1 or 2, wherein ion implantations for field stop formation is conducted only under the to-be-gate electrode area.

4. The method for fabricating MOS transistors as claimed in claim 1 or 2, wherein the sacrificial layer is composed of a

chemical vapor deposition (CVD) oxide layer

5. The method for fabricating MOS transistors as claimed in claim 1 or 2, wherein the sacrificial layer is formed as to have a thickness ranging between 500□ and 1000□.

6. The method for fabricating MOS transistors as claimed in claim 1, wherein the patterning of the sacrificial layer is implemented by wet-etching process.

7. The method for fabricating MOS transistors as claimed in claim 1 or 2, wherein ion for well formation and field stop formation is boron, phosphorous or Arsenic.

8. The method for fabricating MOS transistors as claimed in claim 1 or 2, wherein implant for field stop formation is made at a sufficient energy to form barriers below the source /drain junction.